CLAIM AMENDMENTS

Please amend claims 1, 13, and 20 as follows.

1. (Currently Amended) A system, comprising:

a bus;

first logic having a multiphase phase lock loop to generate a multiphase encoded waveform, the first logic including an input register to receive at least one data word or at least one command/control word, and wherein the command/control word is to indicate whether the multiphase encoded waveform is a data structure or a command/control structure, wherein the bus includes at least one differential transmission line to receive differential signal levels for the multiphase encoded waveform; and

second logic coupled to the first logic to generate differential signal levels representing the multiphase encoded waveform and wherein the second logic further comprises impedance matching circuitry to match impedance of the second logic to the differential transmission line, the impedance matching circuitry comprising:

an operational amplifier;

a first ~~resistance~~ resistor;

a second ~~resistance~~ resistor;

a first ~~capacitance~~ capacitor;

a second ~~capacitance~~ capacitor; and

a transistor,

wherein a first terminal of the first ~~resistance~~ resistor, a first terminal of the second capacitor ~~resistance~~, and a first terminal of the first ~~capacitance~~ capacitor are coupled to a minus input of the operational amplifier, wherein a second terminal of the first ~~capacitance~~ capacitor is coupled to ground, wherein a plus input of the operational amplifier is coupled to Vcc/2, wherein a second terminal of the first ~~resistance~~ resistor, a second terminal of the second ~~capacitance~~ capacitor, and a first terminal of the ~~resistance~~ resistor are coupled to a first terminal of the transistor, wherein a second terminal of the second ~~transistor~~ resistor is coupled to Vcc, wherein an output terminal of the operational amplifier is coupled to a second terminal of the transistor, and wherein a third terminal of the transistor is coupled to ground, and

wherein the second logic is further to drive the multiphase encoded waveform onto the bus.

2. (Canceled).

3. (Canceled)

4. (Canceled).

5. (Previously Presented) The system of claim 1 wherein the input register comprises a first-in-first-out (FIFO) register.

6. (Canceled).

7. (Canceled).

8. (Canceled).

9. (Original) The system of claim 1, further comprising third logic coupled to the bus to receive the multiphase encoded waveform.

10. (Original) The system of claim 9 wherein the third logic includes an amplifier to receive differential signal levels representing the multiphase encoded waveform from the bus and extract the multiphase encoded waveform from the received differential signal levels.

11. (Original) The system of claim 10 wherein the third logic includes a differential delayed lock loop coupled to stretch a multiphase encoded waveform timing to a predetermined length.

12. (Original) The system of claim 11 wherein the third logic includes a register coupled to check data integrity of the multiphase encoded waveform.

13. (Currently Amended) An apparatus, comprising:

a device driver having first logic to generate a multiphase encoded waveform and second logic coupled to the first logic to drive the multiphase encoded waveform onto a bus, wherein the bus includes at least one differential transmission line to receive differential signal levels for the multiphase encoded waveform, wherein second logic includes third logic to generate differential signal levels representing the multiphase encoded waveform, the second logic further to generate differential signal levels representing the multiphase encoded waveform, the second logic further comprising impedance matching circuitry to match impedance of the second logic to the differential transmission line, the impedance matching circuitry comprising:

an operational amplifier;

a first ~~resistance~~ resistor;

a second ~~resistance~~ resistor;

a first ~~capacitance~~ capacitor;

a second ~~capacitance~~ capacitor; and

a transistor,

wherein a first terminal of the first ~~resistance~~ resistor, a first terminal of the second ~~resistance~~ resistor, and a first terminal of the first ~~capacitance~~ capacitor are coupled to a minus input of the operational amplifier, wherein a second terminal of the first ~~capacitance~~ capacitor is coupled to ground, wherein a plus input of the operational amplifier is coupled to Vcc/2, wherein a second terminal of the first ~~resistance~~ resistor, a second terminal of the second ~~capacitance~~ capacitor, and a first terminal of the second ~~resistance~~ resistor are coupled to a first terminal of the transistor, wherein a second terminal of the transistor is coupled to Vcc, wherein an output terminal of the operational amplifier is coupled to a second terminal of the transistor, and wherein a third terminal of the transistor is coupled to ground, and wherein the first logic includes a command/control signal input, wherein a command/control signal on the command/control signal input is to indicate whether the multiphase encoded waveform is a data structure or a command/control structure.

14. (Original) The apparatus of claim 13 wherein the first logic includes a multiphase phase lock loop to generate multiple phases for the multiphase encoded waveform.

15. (Canceled).

16. (Original) The apparatus of claim 14 wherein the first logic includes an input register, coupled to the multiphase phase lock loop, to receive at least one data word or at least one command/control word.

17. (Original) The apparatus of claim 16 wherein the input register comprises a first-in-first-out (FIFO) register.

18. (Canceled).

19. (Canceled).

20. (Currently Amended) An apparatus, comprising:

a device driver to receive a multiphase encoded waveform, having:

an amplifier to receive differential signal levels representing the multiphase encoded waveform from the bus, wherein the bus includes at least one differential transmission line to receive signal levels for the multiphase encoded waveform, and extract the multiphase encoded waveform from the received differential signal levels; [[and]]

a differential delay-lock loop coupled to stretch the received multiphase encoded waveform timing to a predetermined length, wherein the differential delay-lock loop includes logic to align rising edges of the received multiphase encoded waveform to rising edges of a transmitted multiphase encoded waveform; and

logic to generate the differential signal levels representing the multiphase encoded waveform, the logic comprising impedance matching circuitry to match impedance of the logic to the differential transmission line, the impedance matching circuitry comprising:

an operational amplifier;

a first ~~resistance~~ resistor;

a second ~~resistance~~ resistor;

a first ~~capacitance~~ capacitor;

a second ~~capacitance~~ capacitor; and

a transistor,

wherein a first terminal of the first ~~resistance~~ resistor, a first terminal of the second ~~resistance~~ resistor, and a first terminal of the first ~~capacitance~~ capacitor are coupled to a minus input of the operational amplifier, wherein a second terminal of the first ~~capacitance~~ capacitor is coupled to ground, wherein a plus input of the operational amplifier is coupled to Vcc/2, wherein a second terminal of the first ~~resistance~~ resistor, a second terminal of the second ~~capacitance~~ capacitor, and a first terminal of the second ~~resistance~~ resistor are coupled to a first terminal of the transistor, wherein a second terminal of the transistor is coupled to Vcc, wherein an output terminal of the operational amplifier is coupled to a second terminal of the transistor, and wherein a third terminal of the transistor is coupled to ground.

21. (Original) The apparatus of claim 20, further comprising a register coupled to check data integrity of the received multiphase encoded waveform.

22. (Original) The apparatus of claim 21 wherein the register includes logic to extract data bits from the received multiphase encoded waveform and to perform a probability analysis to determine a likelihood of errors.

23. (Canceled).